

Distributed Amplifier Monolithic Microwave Integrated Circuit (MMIC) Design

by John E. Penn

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14. ABSTRACT A very broadband distributed amplifier was designed using a 0.13-μm gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (PHEMT) process from TriQuint Semiconductor. The design and fabrication of this circuit was performed as part of the fall 2011 Johns Hopkins University Monolithic Microwave Integrated Circuit (MMIC) Design Course, taught by the author. The design approach is applicable to very broadband, low noise MMICs that could be used for a variety of radio frequency (RF) and microwave systems.				
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1. Introduction

Very broadband gain can be achieved with distributed amplifiers. The idea of using transmission lines to connect the input and output feeds of parallel gain stages, each with small but broadband gain, was proposed in 1936, but gained popularity after a 1948 paper from Bill Packard (co-founder of Hewlett-Packard Co.) et al. using vacuum tubes for the gain stages (1). While many monolithic microwave integrated circuits (MMICs) are optimized for a particular band to achieve optimal performance, there are many applications that require a broadband response from DC to very high microwave frequencies: such as fiber-optic drivers, electronic warfare (EW) receivers, and other broadband radio frequency (RF) sensors or communications systems.

The distributed amplifier designs documented here were fabricated as part of the Johns Hopkins University (JHU) MMIC Design Course in fall 2011. A similar distributed amplifier design using TriQuint's TQPED 0.5- μm gallium arsenide (GaAs) pseudomorphic high electron mobility transistors (PHEMTs) was designed and fabricated along with the student designs for the 2006 JHU MMIC Design Course. That earlier 0.5- μm PHEMT design worked well from 1 to 10 GHz and was published in the November 2007 issue of *Microwaves and RF* (2). This distributed amplifier design uses a much higher frequency TriQuint TQP13 0.13- μm PHEMT process, resulting in more than two decades of gain bandwidth. Depending on the frequency, space available, etc., the "transmission line" feeds of the distributed amplifier can be distributed, typically microstrip, or the feed can be a lumped element transmission line equivalent (3). This distributed amplifier uses the lumped element transmission line equivalent approach, but could have used microstrip line feeds.

2. Distributed Amplifier Design

In the distributed amplifier, a signal travels down the input transmission line feeding each of several parallel gain stages (figure 1). Each gain stage has a small amount of gain, but the gain is broadband, summing up at the output transmission line to provide an amplified signal. Typically, there is a cutoff frequency limiting the number of stages that can be paralleled. Depending on frequency, size available, device characteristics, etc., it may be beneficial to replace the distributed transmission line with a lumped element equivalent of a transmission line, which uses the input and output capacitance of a transistor gain stage tuned to inductances in the feed lines to control the impedances and gain over a broad operating band (figure 2).

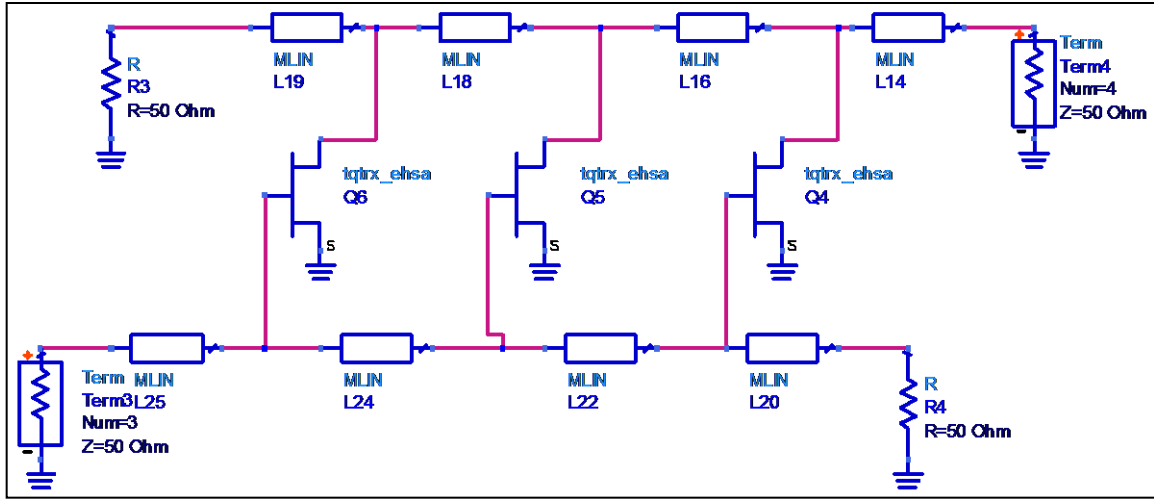


Figure 1. Distributed amplifier with three stages.

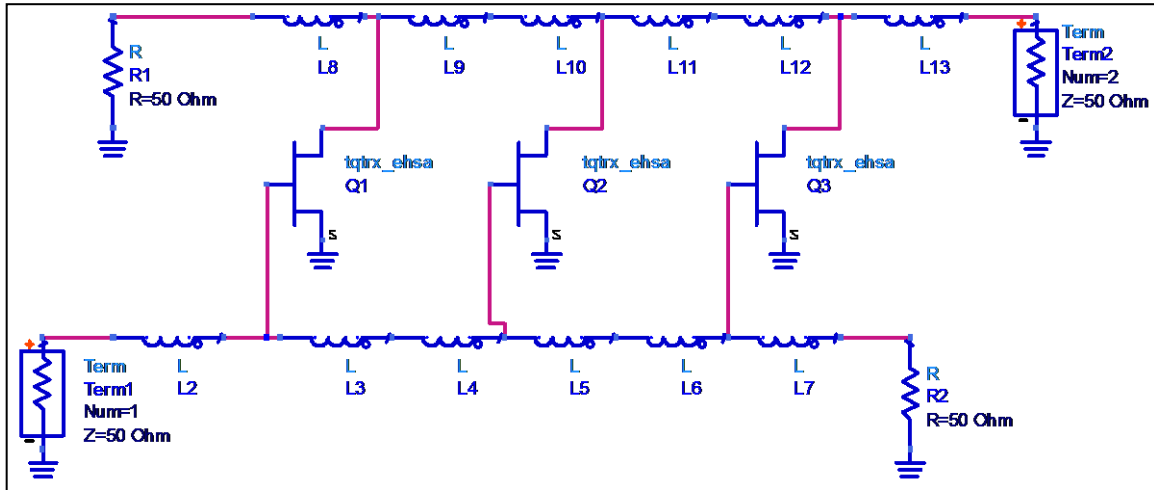


Figure 2. Distributed amplifier with three stages using lumped element feeds.

The drain (output) and gate (input) feed lines of the distributed amplifier design are terminated in a 50-ohm resistor. This tends to dissipate half the output power, resulting in lower efficiency. There is a method using tapered output lines to try and reduce this 3-dB loss, but the implementation can be difficult to achieve, except in simulations using ideal elements. In the lumped element approach, the inductances in the gate and drain lines are adjusted to create a matched 50-ohm input and output impedance over a broad range with relatively flat gain. The number of transistor stages and the size of the device can be tuned to optimize the performance. Figure 3 shows the good agreement between simulations of the previous 0.5- μm PHEMT distributed amplifier of 2006 and measurements of the fabricated circuit.

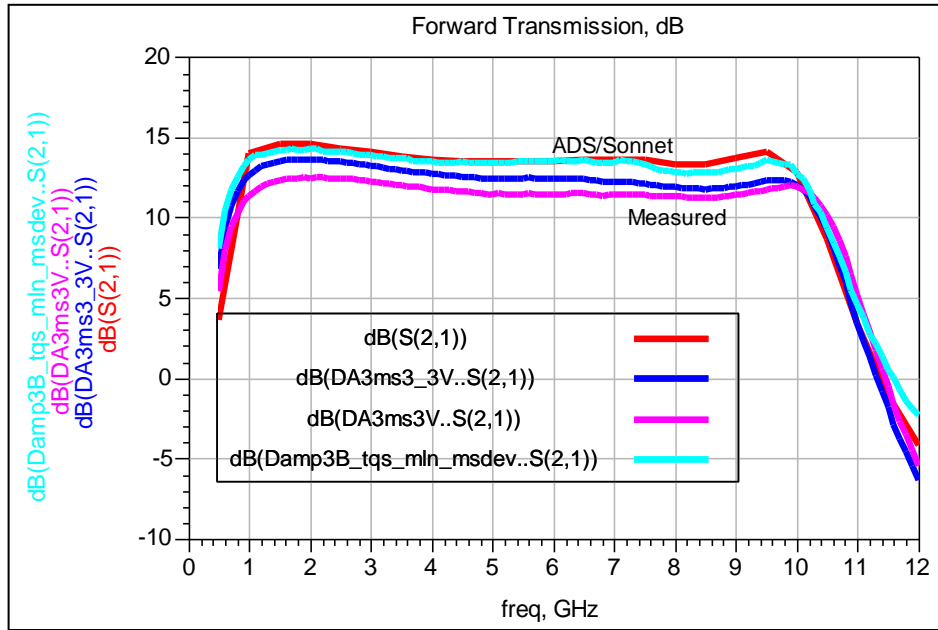


Figure 3. Gain measurements vs. simulations for a 0.5- μ m PHEMT distributed amplifier (2006).

Using a much higher frequency 0.13- μ m PHEMT process from TriQuint, an updated distributed amplifier was designed. A lumped element approach was maintained with some initial tuning of the transistor size along with the drain and gate feed inductors to obtain a first cut of the amplifier design. Then, ideal elements were replaced with actual “lossy” passive MMIC elements and re-tuned based on the simulations. Two nearly similar versions of the distributed amplifier were created with one subtle difference. The first design uses a spiral inductor connected in parallel to the 50-ohm drain termination, which reduces DC power consumption. This limits the low end frequency response to about 1 GHz, and, as the design has two decades of bandwidth, the resonance of this inductor causes a slight ripple in the gain (~ 20 GHz), as shown in the preliminary S-parameter simulation of figure 4. The simulation compares the amplifier using TriQuint’s TQP13 passive elements, without interconnect, versus ideal lumped elements. In the alternate layout, the DC supply current through the 50-ohm drain termination reduces the power efficiency, but allows gain at much lower frequencies than supplying DC current through the inductor. Figure 5 shows a similar simulation comparing the alternate DC to a 30-GHz amplifier using TriQuint’s TQP13 passive elements, without interconnect, versus ideal lumped elements. The preliminary schematic using ideal elements is shown in figure 6, with the “lossy” TQP13 schematic in figure 7. Again, the only difference in the two designs is the DC supply in the upper top left of the schematics. Originally, an external DC gate bias was to be supplied, but it can be difficult to make a broadband DC supply for a distributed amplifier over two decades of bandwidth. The gate (input) DC supply was simplified by terminating the 50-ohm load resistor to a substrate ground via to provide a fixed 0 V “ V_{gs} ”. This removes the flexibility of controlling the drain current, but it also removes any resonances and potential

instabilities that might be created in the gate DC bias supply. For these TQP13 PHEMT devices, 0 V “V_{gs}” bias provides good gain, and good noise figure at a moderate DC power consumption.

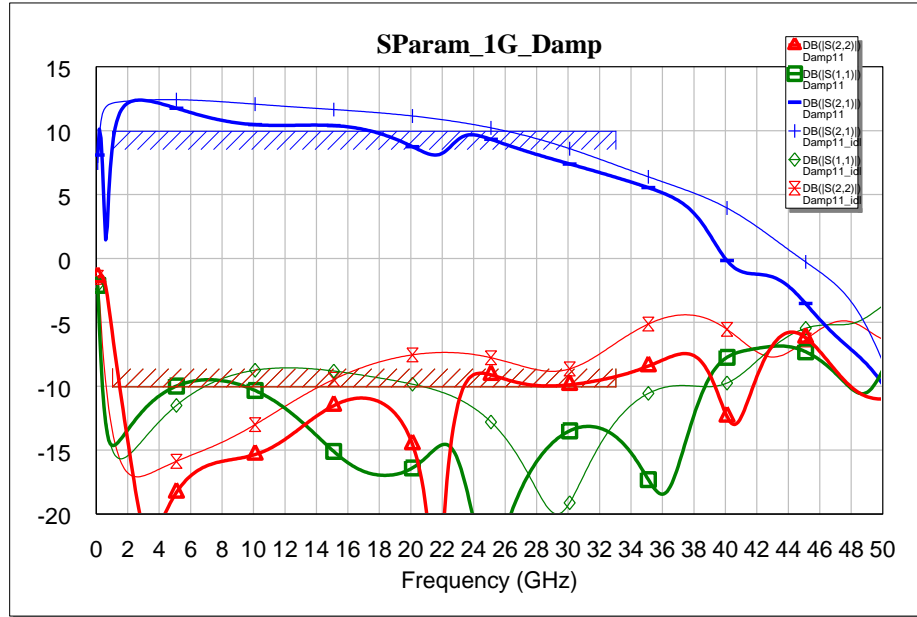


Figure 4. S-parameter performance of an ideal distributed amplifier design (thin lines) vs. the TriQuint elements (thick lines).

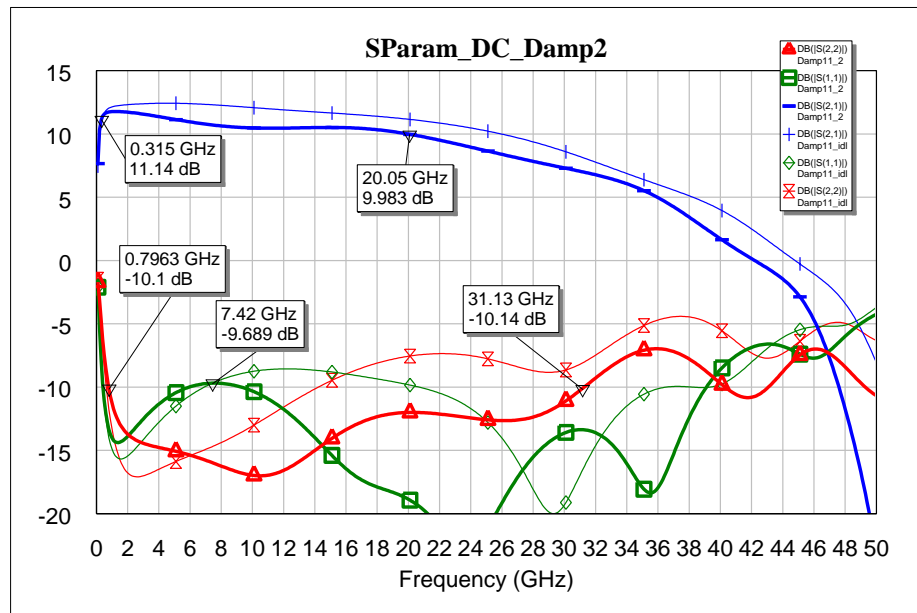


Figure 5. S-parameter performance of an ideal distributed amplifier design (thin lines) vs. the DC to 30 GHz amplifier with TriQuint elements (thick lines).

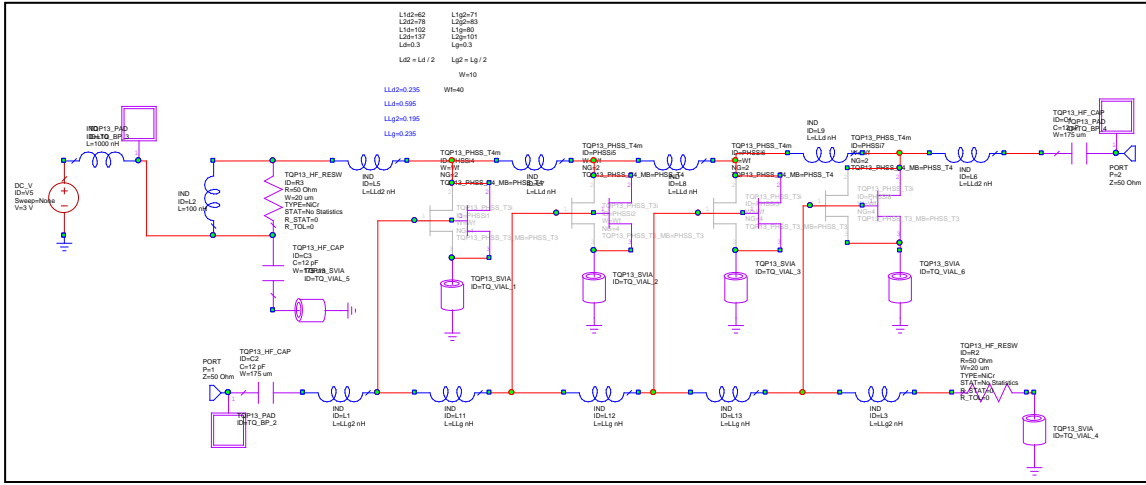


Figure 6. Schematic of an ideal distributed amplifier design.

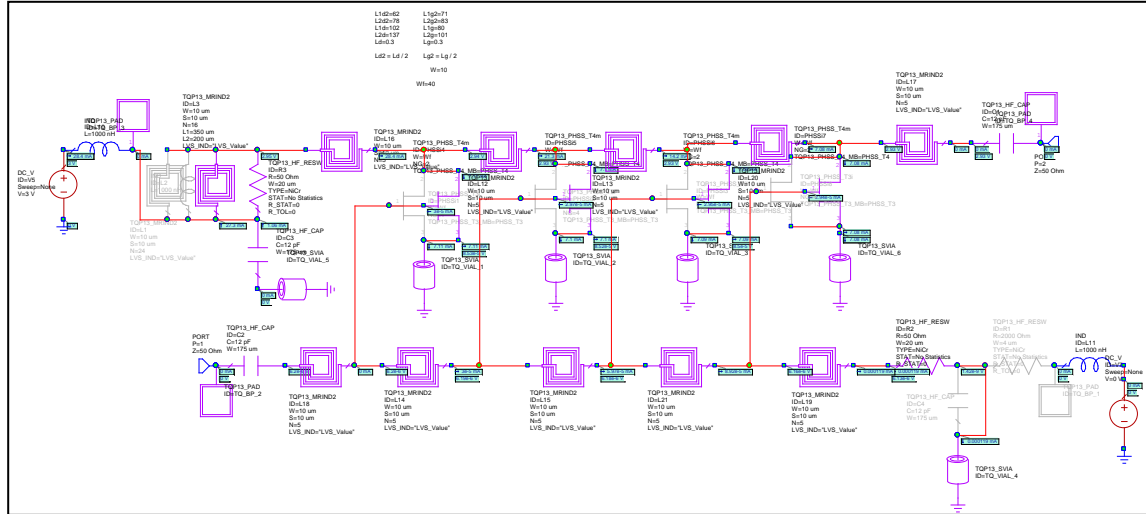


Figure 7. Schematic of the TriQuint element distributed amplifier design.

The layout of both distributed amplifiers on a 54x54 mil die is shown in figure 8. At the top of the die is the DC to 30-GHz distributed amplifier and the bottom of the die is the 1 to 30 GHz version.

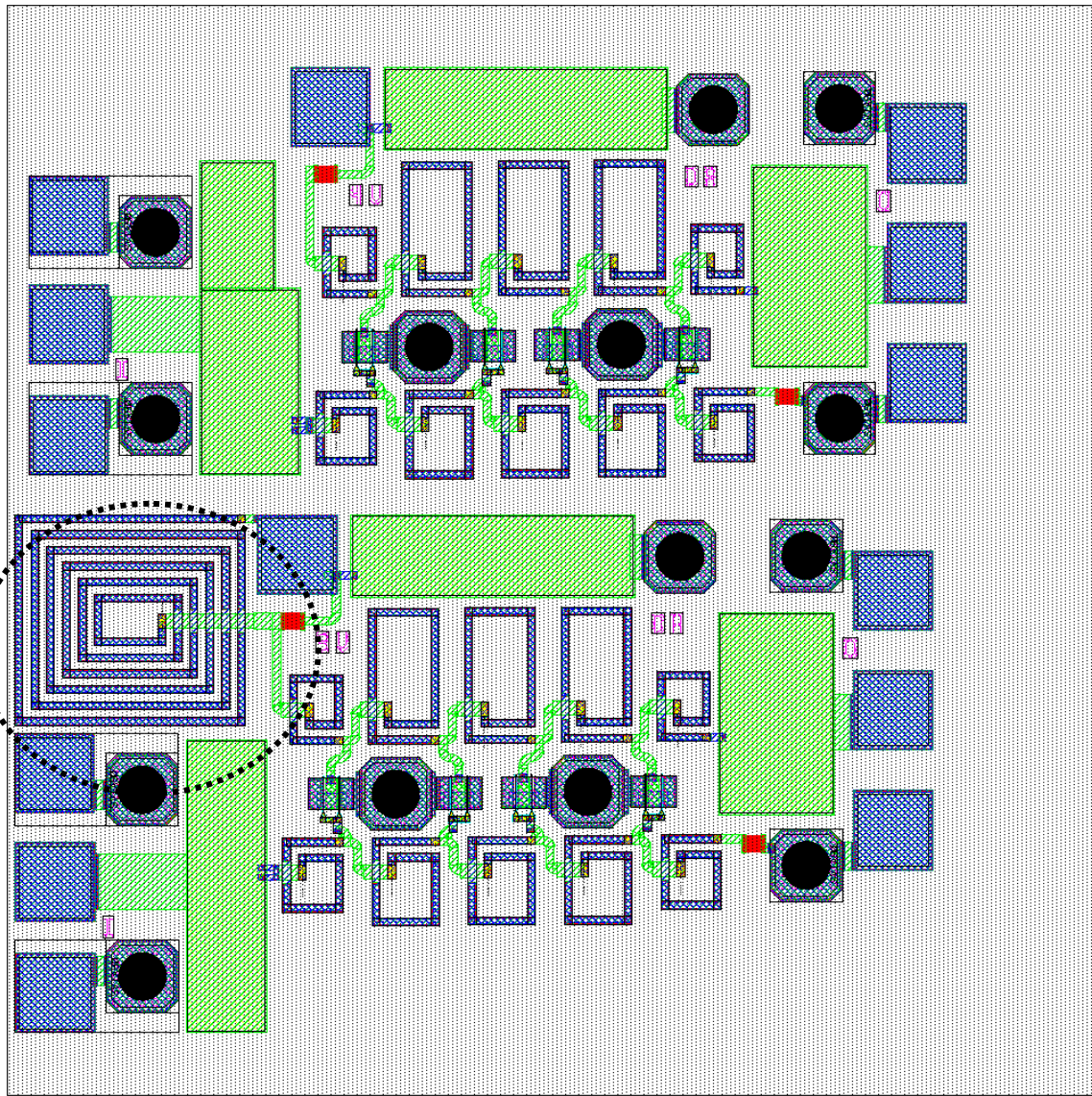


Figure 8. Layout plot of the TriQuint element distributed amplifier designs on a 54x54 mil die.

3. Sonnet Simulations

Both designs are essentially identical except for the spiral inductor in the drain bias. Sonnet was used to electromagnetically simulate the layout, which showed a potential stability problem at higher frequency (~ 30 GHz) (figures 9 and 10). One concern is the relatively large decoupling

capacitor on the drain DC bias and its relatively close spacing to the spiral inductors of the drain feed line. To improve the design, the 12-pF large capacitor was split into two 6-pF capacitors to allow a shorter path to ground for the higher frequency operation while maintaining a 12-pF total capacitance for the lower frequency operation. Also, the capacitor was moved further away from the spiral inductors of the drain feed to reduce parasitic coupling. Lastly, 5-ohm resistors on the drain were added in the simulation, which significantly reduced the previous stability problem (~30 GHz) (figures 11 and 12). A modified layout with the stabilizing resistors and modified capacitor is shown in figure 13 for the same 54x54 mil Die.

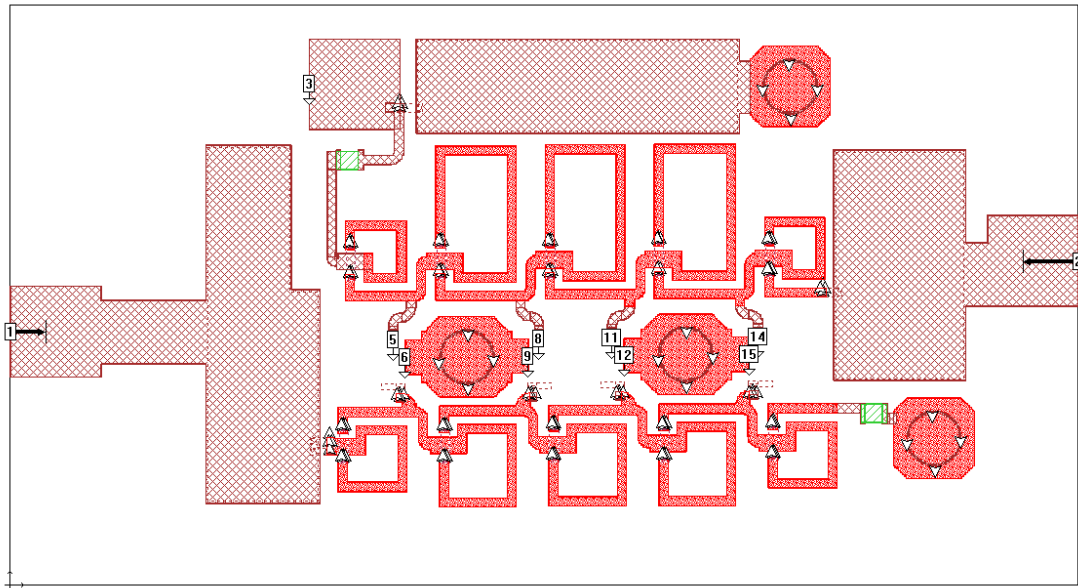


Figure 9. Sonnet electromagnetic (EM) layout plot of the DC-30 GHz distributed amplifier.

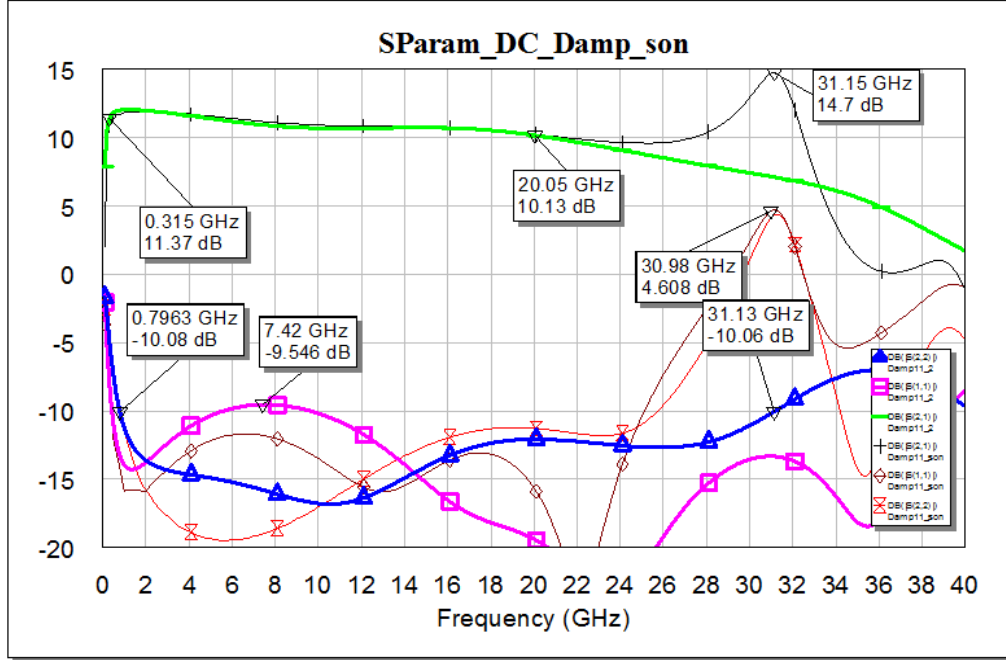


Figure 10. Sonnet EM simulation of the DC-30 GHz distributed amplifier with a 31-GHz stability problem.

The current view of Sonnet can help give insight into the parasitic coupling of the actual layout. At 2 GHz, the electric field strength around the two 6-pf capacitors is approximately symmetric but at 30 GHz, the field is stronger for the left side of the first 6-pf capacitor, particularly at the substrate via a ground connection. Propagation tends to take the shortest path, which led to the premise that at higher frequencies the smaller 6-pf capacitor would be better than a much larger 12-pf capacitor. The larger 12-pf capacitor would also have a lower resonant frequency. Some more simulations could be beneficial to determine a more optimal approach. Figures 14, and 15 show the field strength around the two 6-pf capacitors at 2 and 30 GHz using the current viewer in Sonnet. Likewise, the original layout with a single 12-pf capacitor is shown in figures 16 and 17 for comparison.

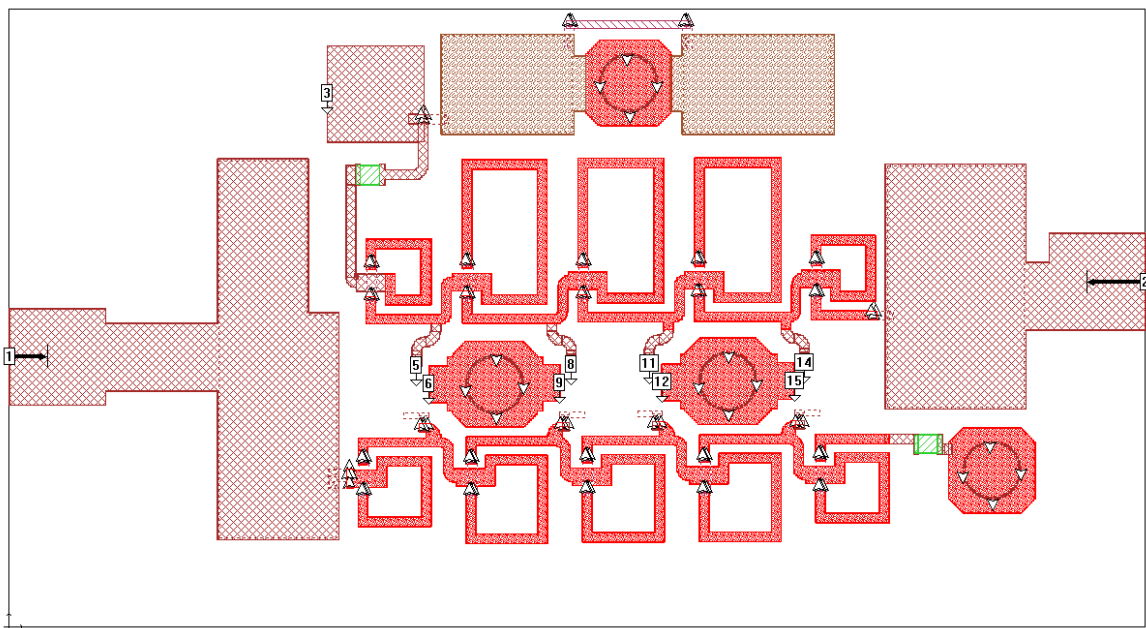


Figure 11. Sonnet EM layout plot of the DC-30 GHz distributed amplifier “redo.”

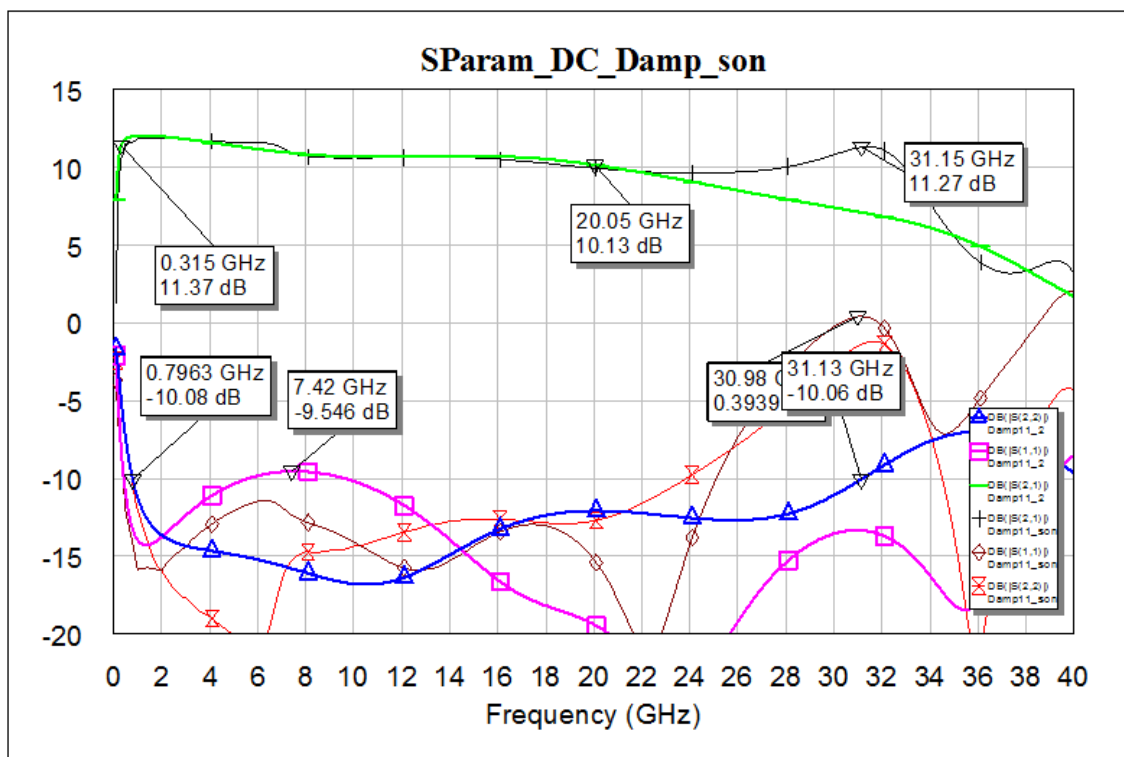


Figure 12. Sonnet EM simulation of the DC-30 GHz distributed amplifier “redo” with improved stability.

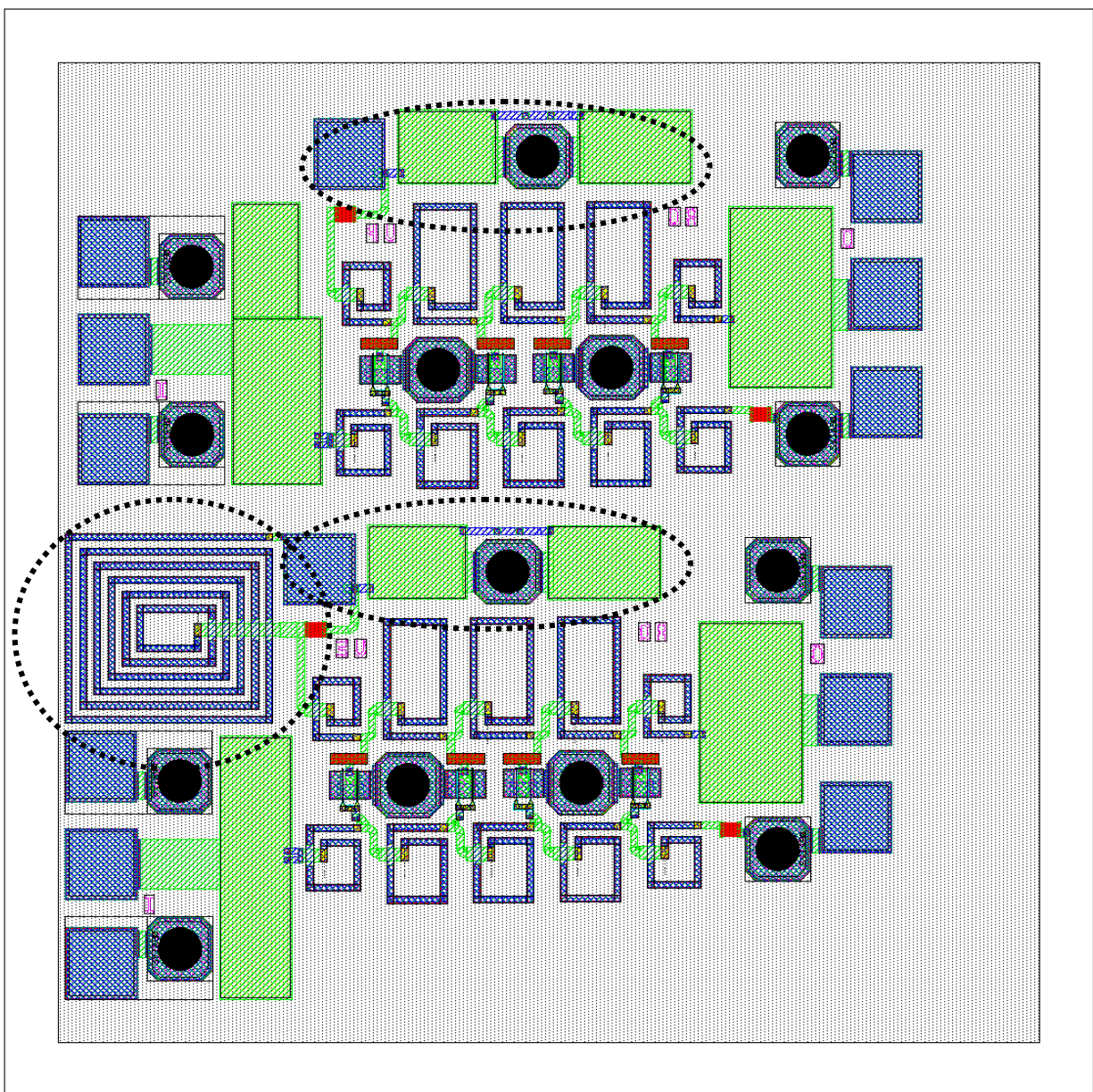


Figure 13. Layout plot of the modified TriQuint element distributed amplifier designs (54x54 mil).

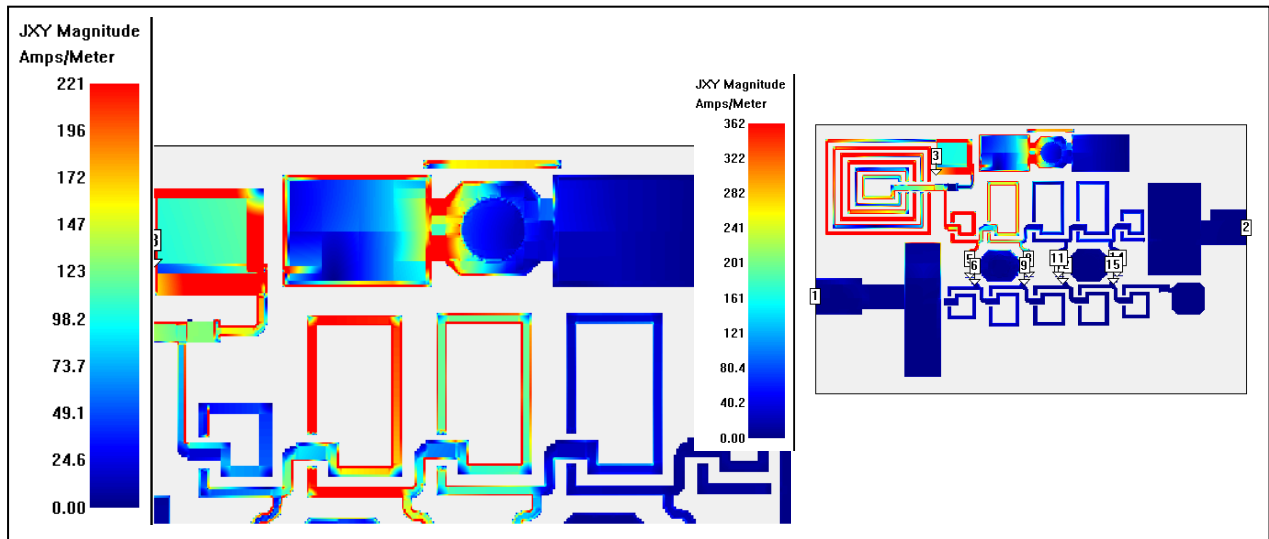


Figure 14. Sonnet EM current plot of the modified distributed amplifier at 30 GHz.

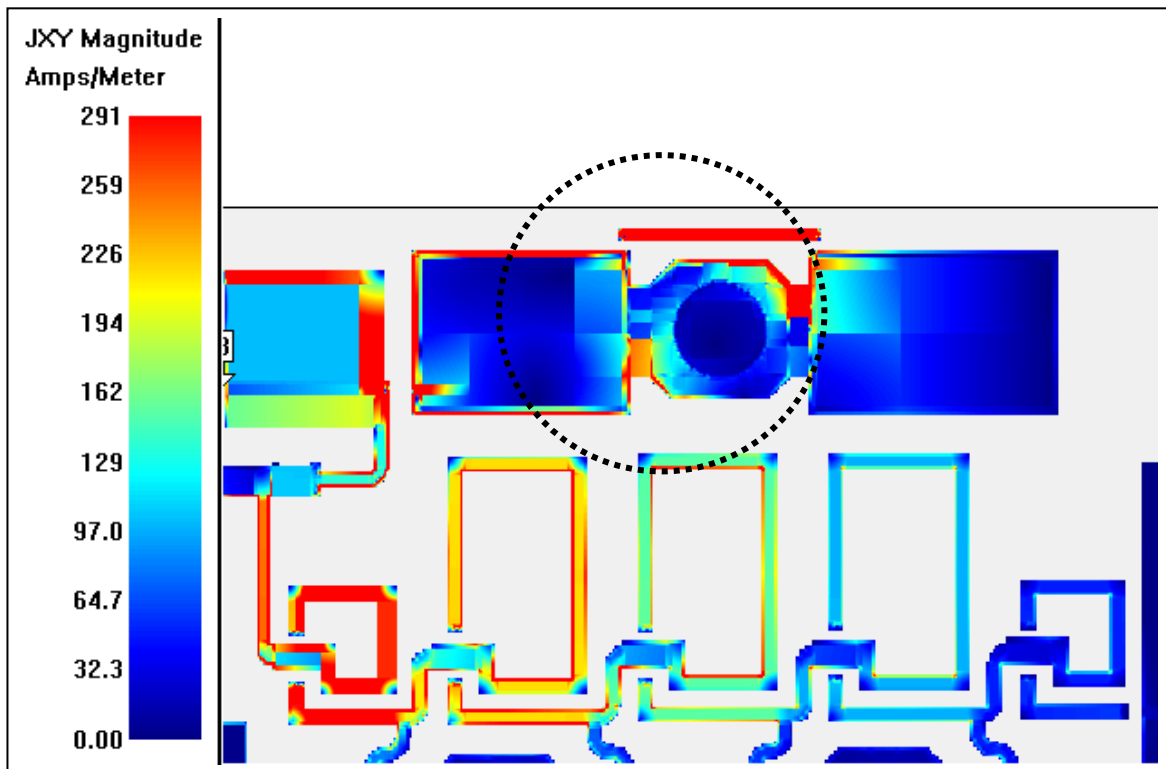


Figure 15. Sonnet EM current plot of the modified distributed amplifier at 2 GHz.

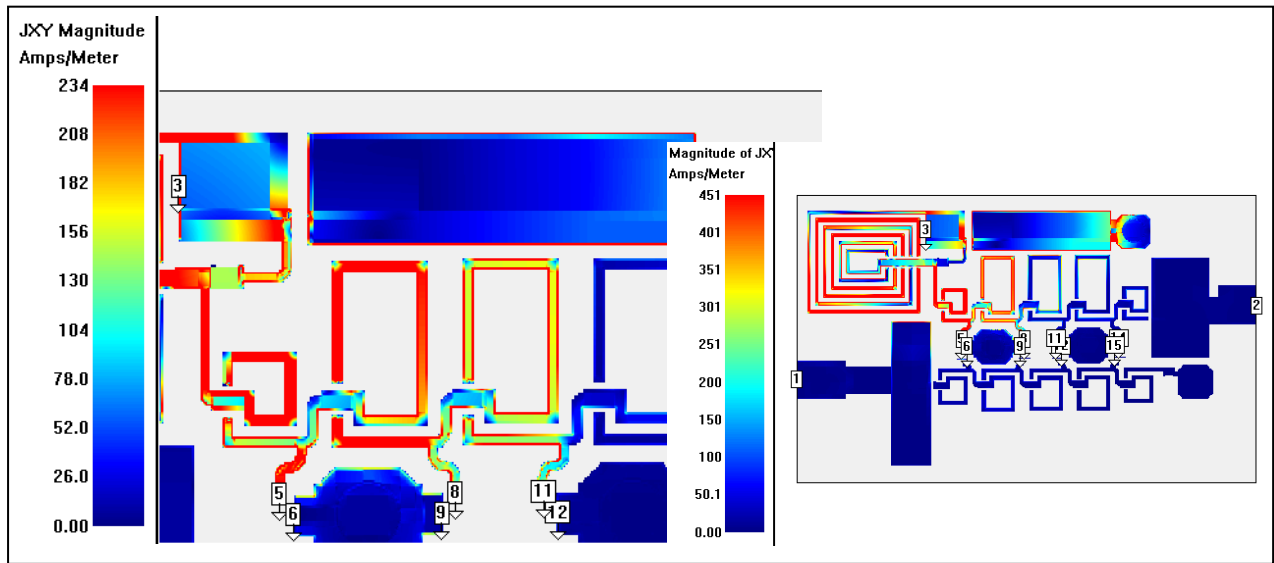


Figure 16. Sonnet EM current plot of the original distributed amplifier at 30 GHz.

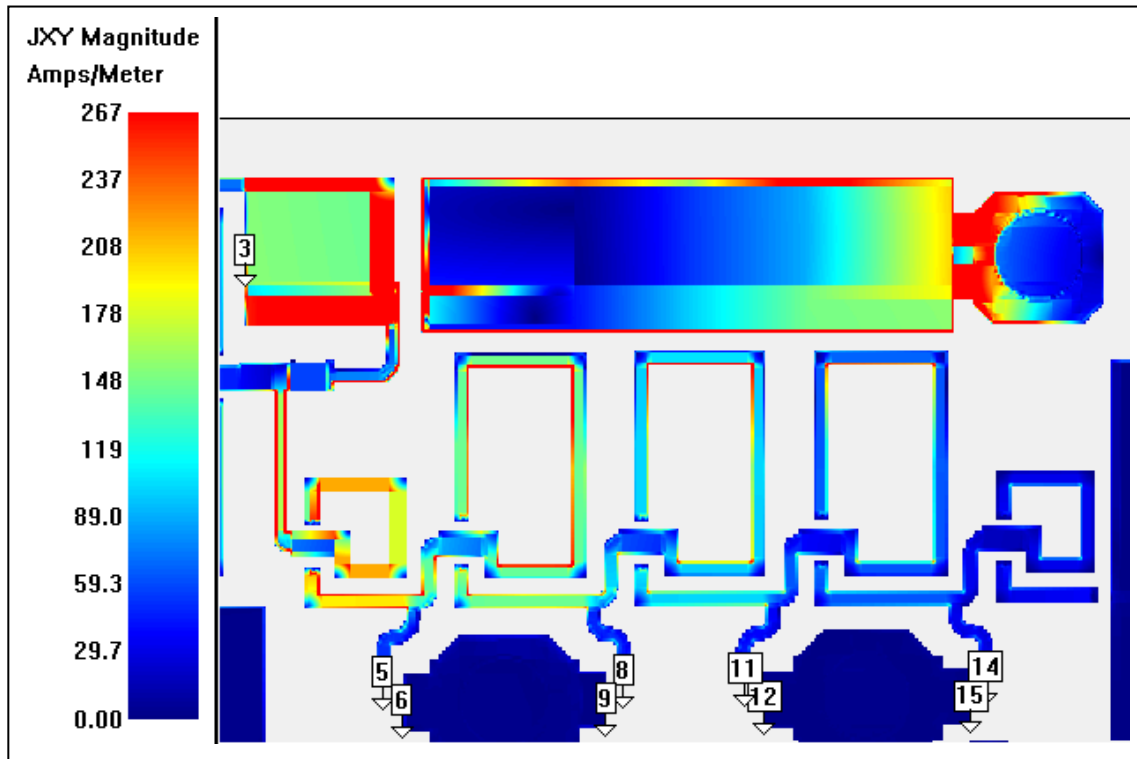


Figure 17. Sonnet EM current plot of the original distributed amplifier at 2 GHz.

4. Testing

When the fabricated student designs were returned, unfortunately, the original distributed amplifier designs were inadvertently submitted, rather than the modified designs. During testing, both distributed amplifiers showed promise at lower bias voltages and at their nominal design voltages, but appeared to be conditionally stable at certain intermediate voltages. These oscillations appeared to be well above 45 GHz, but would disappear near the nominal design voltages of 3 V (1–30 GHz) and 4 V (DC–30 GHz), and higher DC biases. Figure 14 shows a plot of measured performance for the two designs, which differ only by the DC supply bypass inductor. Noise figure and gain was measured at 4-V bias for the DC–30 GHz version, showing slightly higher noise figure than expected, but decent, at 3 dB from 15 to 26 GHz (highest frequency measured) (figure 18). Simulations of noise figure show a similar shape but were expected to be better, closer to 2 dB (figure 19). Efficiency and output power versus input power are plotted in figure 20 for the more efficient 1–30 GHz amplifier at 10 GHz showing a respectable 20% power added efficiency (PAE) at 2-dB gain compression. The simulated performance is reasonably similar as shown in figure 21. Likewise, the performance of the less efficient DC–30 GHz distributed amplifier is shown in figure 22. Those measurements are also very similar to the simulations shown in figure 23. A three-dimensional (3-D) view of the layout of the distributed amplifier (1–30 GHz) is shown in figure 24.

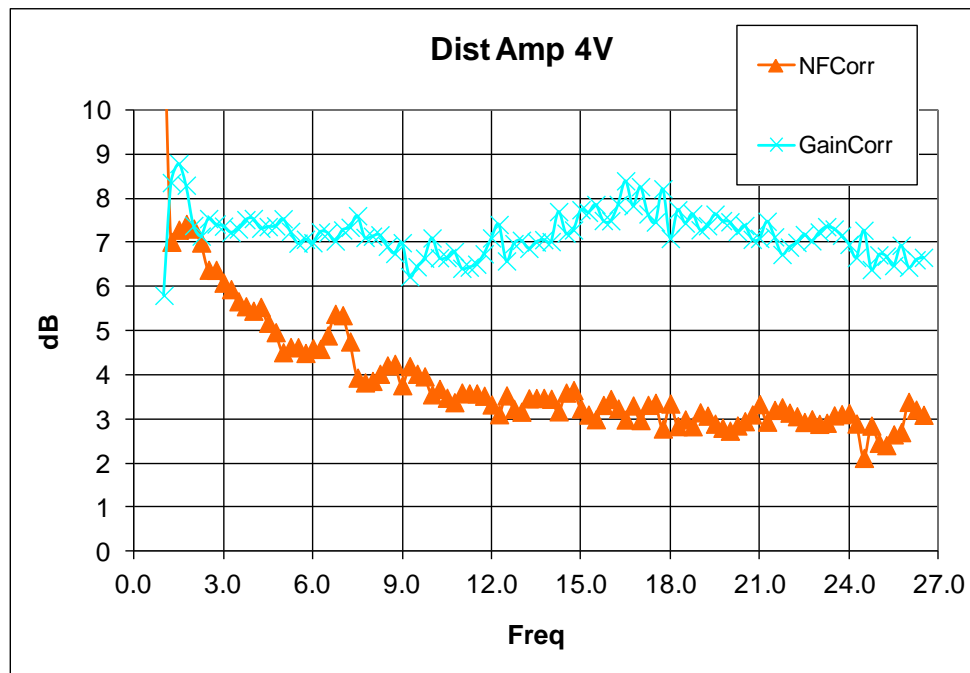


Figure 18. Noise figure and gain performance of the DC–30 GHz distributed amplifier design.

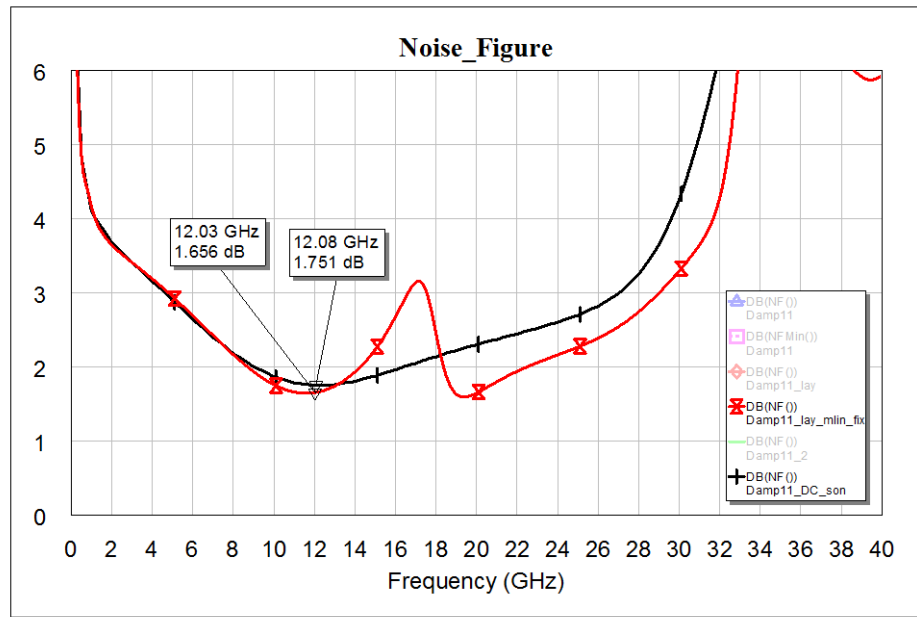


Figure 19. Simulated noise figure: distributed amplifier designs (red-1G+, black-DC+).

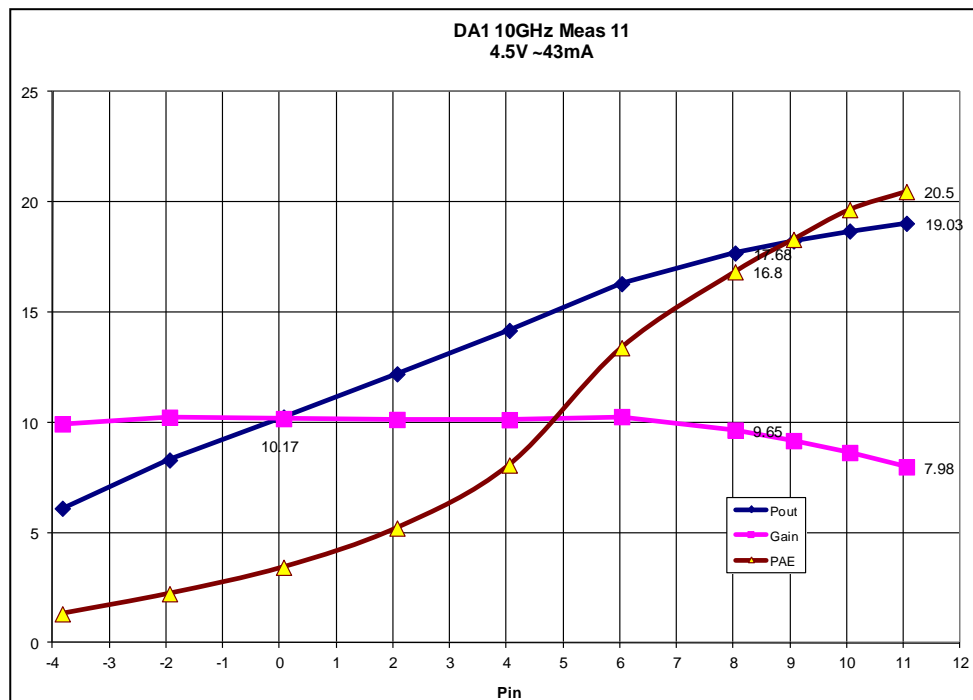


Figure 20. Measured output power, gain, and efficiency performance of the 1–30 GHz distributed amplifier design at 10 GHz.

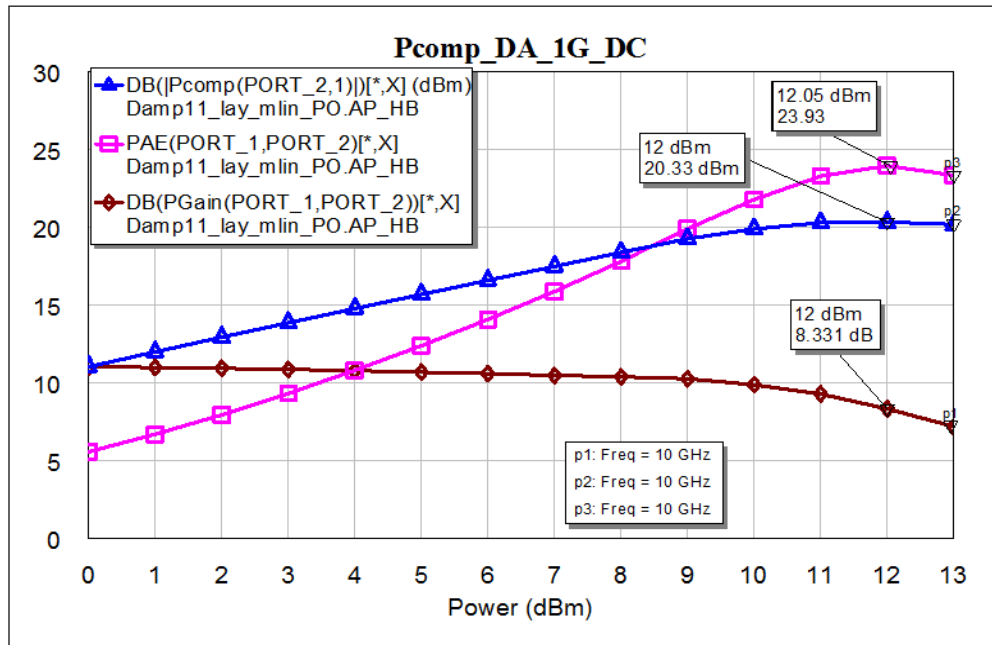


Figure 21. Simulated output power, gain, and efficiency performance of the 1–30 GHz distributed amplifier design at 10 GHz.

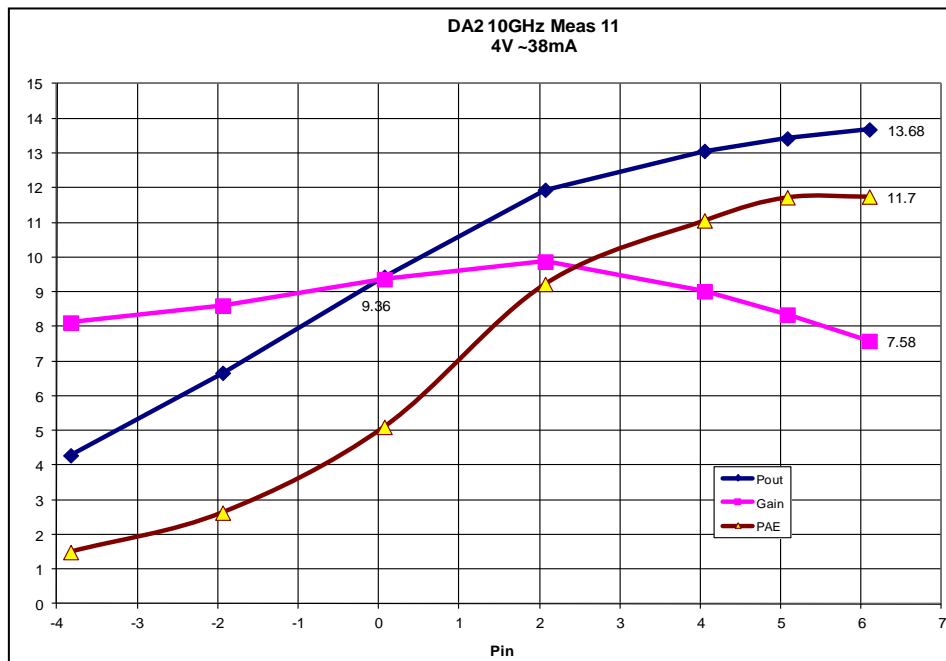


Figure 22. Measured output power, gain, and efficiency performance of the DC-30 GHz distributed amplifier design at 10 GHz.

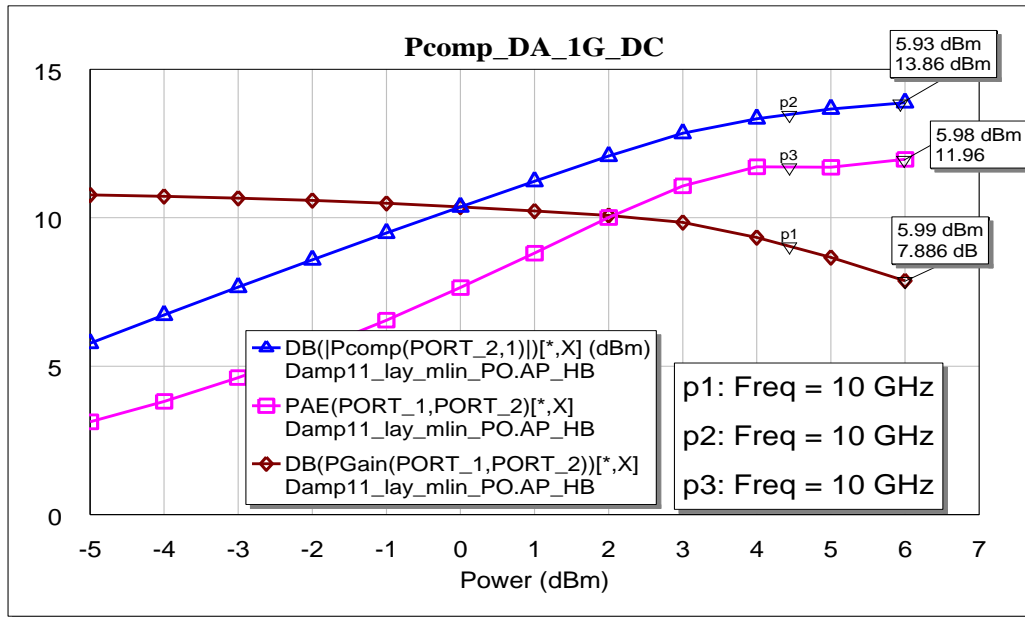


Figure 23. Simulated output power, gain, and efficiency performance of the DC-30 GHz distributed amplifier design at 10 GHz.

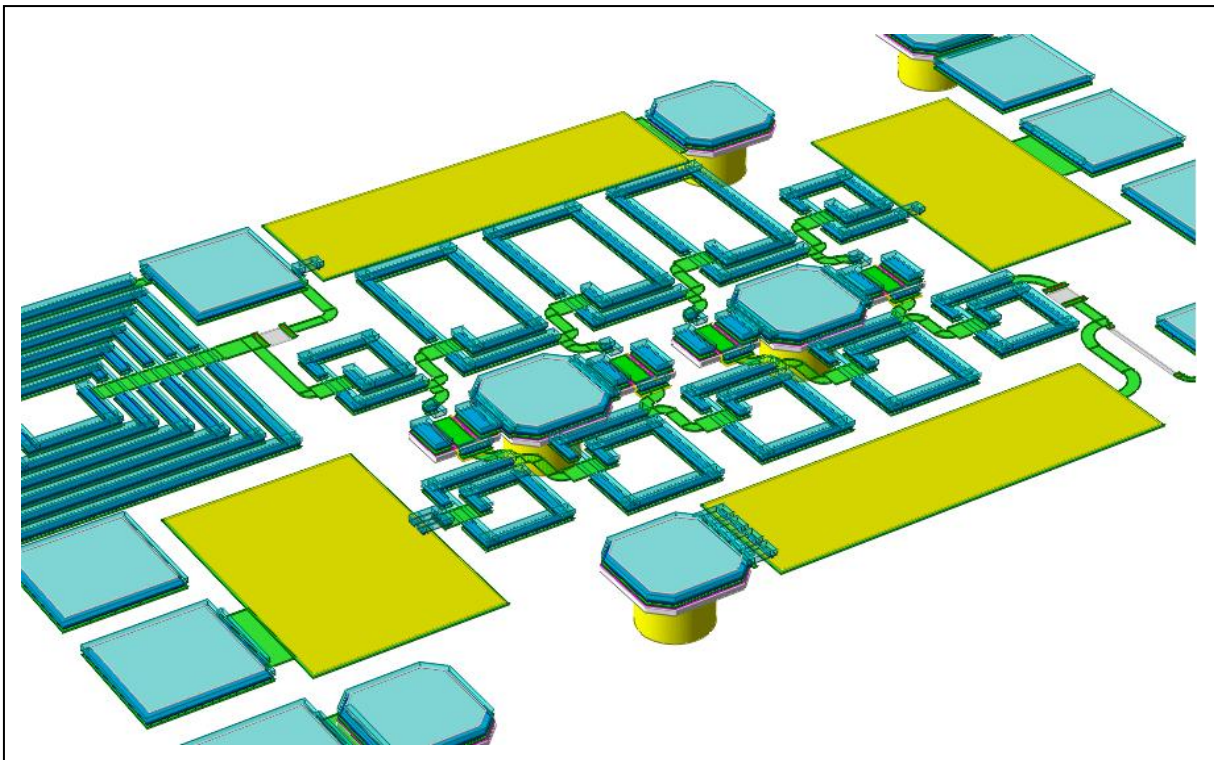


Figure 24. A 3-D view of the MMIC distributed amplifier layout (1 GHz+).

5. Conclusion

Both versions of the distributed amplifier worked well, with the 1–30 GHz version providing higher output power and efficiency, while the DC–30 GHz version had gain below 1 GHz and avoided the gain ripple from the resonance due to the DC bypass inductor. There appeared to be some conditional stability concerns, which might make the design less robust over process variation in repeat fabrications. Hopefully, there will be a future fabrication of the modified designs to test for improved stability.

6. References

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2. Penn, J. E. Designing MMIC Distributed Amplifiers. *Microwaves & RF* **November 2007**.
3. Penn, J. E. Convert Distributed MICs to MMICs. *Microwaves & RF* **July 2003**.

List of Symbols, Abbreviations, and Acronyms

3-D	three-dimensional
EM	electromagnetic
EW	electronic warfare
GaAs	gallium arsenide
JHU	Johns Hopkins University
MMIC	monolithic microwave integrated circuit
PAE	power added efficiency
PHEMTs	pseudomorphic high electron mobility transistors
RF	radio frequency

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